

**WHAT IS CLAIMED IS:**

1           1. A memory management unit configured to receive a virtual address and  
2 provide a corresponding physical address, the memory management unit comprising:  
3           a storage containing one or more virtual address-to-physical address translations;  
4           conversion logic to generate a modified virtual address from the virtual address;  
5           and  
6           a page table walk unit configured to convert the modified virtual address into the  
7           corresponding physical address.

8           2. The memory management unit as recited in Claim 1, wherein the conversion  
9 logic is configured to replace one or more bits of the virtual address with a process  
10 identifier if the one or more bits comprises a predetermined value.

11           3. The memory management unit as recited in Claim 2, wherein the  
12 predetermined value is zero.

13           4. The memory management unit as recited in Claim 1, wherein the memory  
14 management unit is configured to receive the virtual address from an arithmetic logic  
15 unit.

16           5. The memory management unit as recited in Claim 1, wherein the memory  
17 management unit is configured to receive the virtual address from an incrementor.

18           6. The memory management unit as recited in Claim 1, wherein the virtual  
19 address comprises a data address.

20           7. The memory management unit as recited in Claim 1, wherein the virtual  
21 address comprises an instruction address.

22           8. The memory management unit as recited in Claim 1, wherein the one or more  
23 virtual address-to-physical address translations are invalidated upon updates to a process  
24 identifier.

25           9. The memory management unit as recited in Claim 1, wherein only virtual  
26 address-to-physical address translations having a virtual address portion with one or more  
27 bits equal to a predetermined value are invalidated upon updates to a process identifier.

28           10. The memory management unit as recited in Claim 1, wherein the storage is  
29 configured to store one or more most recently generated virtual address-to-physical  
30 address translations.

31           11. A system comprising:  
32           an antenna;  
33           a memory; and  
34           a processor coupled to the antenna and memory, the processor comprising:  
35                 an address generation unit; and  
36                 a memory management unit configured to receive a virtual address from  
37                 the address generation unit and provide a corresponding physical address,  
38                 the memory management unit comprising:  
39                         a storage containing one or more virtual address-to-physical  
40                         address translations;

41 conversion logic to generate a modified virtual address from the  
42 virtual address; and  
43 a page table walk unit configured to convert the modified virtual  
44 address into the corresponding physical address.

45 12. The system as recited in Claim 11, wherein the conversion logic is configured  
46 to replace one or more bits of the virtual address with a process identifier if the one or  
47 more bits are equal to a predetermined value.

48 13. The system as recited in Claim 11, wherein the address generation unit  
49 comprises an arithmetic logic unit.

50 14. The system as recited in Claim 11, wherein the address generation unit  
51 comprises an incrementor.

52 15. The system as recited in Claim 11, wherein the one or more virtual address-to-  
53 physical address translations are invalidated upon updates to a process identifier.

54 16. The system as recited in Claim 11, wherein only virtual address-to-physical  
55 address translations having a virtual address portion with one or more bits equal to a  
56 predetermined value are invalidated upon updates to a process identifier.

57 17. A method comprising:  
58 receiving a virtual address;  
59 determining if the virtual address has a translation to a physical address in a  
60 storage;

61 if not, generating a modified virtual address from the virtual address; and  
62 translating the modified virtual address into a physical address.

63 18. The method as recited in Claim 17, wherein generating the modified virtual  
64 address comprises replacing one or more bits of the virtual address with a process  
65 identifier if the one or more bits are equal to a predetermined value.

66 19. The method as recited in Claim 17, wherein translating the modified virtual  
67 address comprises performing a page table walk.

68 20. The method as recited in Claim 17, further comprising invalidating all  
69 translations in the storage if a process identifier changes.

70 21. The method as recited in Claim 17, further comprising invalidating only  
71 translations in the storage having a virtual address portion that has one or more bits equal  
72 to a predetermined value.

73 22. The method as recited in Claim 17, further comprising placing any generated  
74 translations into the storage.

75 23. The method as recited in Claim 17, wherein the virtual address is a data  
76 address.

77 24. The method as recited in Claim 17, wherein the virtual address is an  
78 instruction address.